High-Yield Design Technologies for InAlAs/InGaAs/InP-HEMT Analog-Digital ICs

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Abstract— **Sixty-GHz-band two-stage monolithic low-noise amplifiers and ultrahigh-speed SCFL static frequency dividers have been fabricated using the same InAlAs/InGaAs/InP HEMT process. This process assures uniformity by taking advantage of a 0.1-μm T-shaped gate and an InP recess-etch stopper. Circuits are designed with priorities on stable operation, high yield, and uniformity. For the low-noise amplifier, the stabilization is optimized so as to minimize noise for the design gain while maintaining stability at all frequencies. The resultant amplifiers show a fabrication yield of 75% and at 62 GHz have a noise figure of 4.3 $\pm$ 0.19 dB and a gain of 11.8 $\pm$ 0.25 dB. For the frequency divider, the load resistance is set to be large enough to assure stable operation (circuit simulation shows that increasing the load resistance has little effect on the maximum toggle frequency). Frequency dividers designed with the optimum load resistance for stable and high-speed operation show a fabrication yield of 63% and have a maximum toggle frequency of 36.7 $\pm$ 0.55 GHz. These results demonstrate the feasibility of using this HEMT process to monolithically integrate analog and digital circuits on one chip.**

I. Introduction

InAlAs/InGaAs/InP HEMT's have demonstrated ultrahigh-speed and low-noise performance superior to that of any other transistor, including the highest f_T (340 GHz, as reported in [1]), the highest f_{max} (600 GHz, as reported in [2]), the lowest noise figure at room temperature [3], and the highest efficiency at millimeter-wave frequencies [1], [4]. Because of these excellent high-frequency characteristics, InAlAs/InGaAs/InP HEMT's have been applied to various monolithic microwave integrated circuits (MMIC), such as low-noise amplifiers [5]–[8], high-power amplifiers [9], traveling-wave amplifiers [10], mixers [11], oscillators [12], and the integration of these kinds of analog circuits (receivers, as reported in [13]). We also reported monolithic low-noise amplifiers (LNA) for 26-, 40-, and 50-GHz bands [14]–[16] and a distributed baseband amplifier for dc to 90 GHz [17] as analog IC's. In the application to digital IC's, the toggle frequency of static frequency dividers using these HEMT's remained 26.7 GHz [18] because of immaturity of the fabrication process. Recently, we have developed the first successful InAlAs/InGaAs/InP-HEMT process for digital IC's by introducing an InP recess-etch stopper [19], [20] grown by MOCVD. This process enabled us to make a source-coupled-FET-logic (SCFL) [21] static frequency divider operating at 40.4 GHz [20]. The next step, integrating analog and digital circuits on one chip, will make it possible to build one-chip phase-locked-loop IC's for frequency synthesizers and to build, for optical transmission systems, monolithic front-end IC's including a preamplifier and decision circuit. The monolithic integration of such circuits can also reduce the degradation of circuit performance due to the implementation to fixtures and lower the cost of circuit modules. Moreover, in the millimeter-wave region, interfacing between analog and digital circuits becomes increasingly difficult as the frequency increases. This integration is therefore considered to be essential for the future ultrahigh-speed radio- and optical-transmission systems. It requires, however, that both the analog and digital IC's be fabricated using the same IC process. It is also necessary to improve yield and uniformity while maintaining the performance of both kinds of IC's.

This paper reports a study on the feasibility of monolithically integrating analog and digital circuits by using the InAlAs/InGaAs/InP HEMT process. An MMIC-LNA was used as the analog test circuit so that we could evaluate the fundamental performance of analog IC's (i.e., so we could evaluate their gain and noise characteristics). An SCFL frequency divider was used as the digital test circuit because this kind of circuit reveals the basic operations of SCFL gates. The applicability of the HEMT process to both kinds of IC's is evaluated separately here by presenting the yield and uniformity, as well as the performance, for each kind.

II. InAlAs/InGaAs/InP HEMT Technologies

InAlAs/InGaAs modulation-doped heterostructure lattice-matched to InP substrate was grown by MOCVD. Fig. 1 shows the cross section of a HEMT with a gate length of 0.1 μm. Although mushroom-shaped gates formed with a multilayer resist system are commonly used, their production requires critical control of EB exposure and development. Therefore, to increase productivity, direct EB delineation was used to form a T-shaped-gate for the gate footprint and optical lithography was used to form the top part of the gate electrode [22]. To ensure uniformity of gate-recess depth, an InP layer was inserted into the InAlAs barrier layer as a gate-recess-etch stopper. The InP etch stopper is compatible with the n^+-InGaAs/n^+-InAlAs cap layer used for nonalloyed ohmic contact [22] in the fabrication process. The interconnection lines, which were developed for the conventional MMIC process, were composed of one-layer

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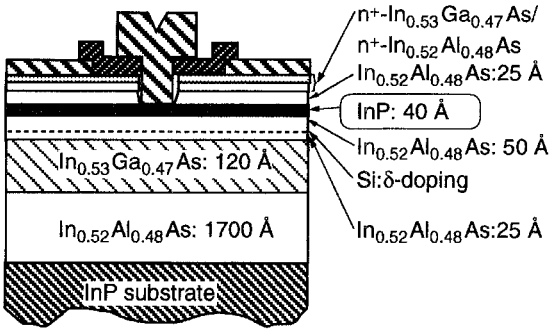


Fig. 1. Cross section of an InAlAs/InGaAs/InP HEMT with an InP recess-etch stopper.

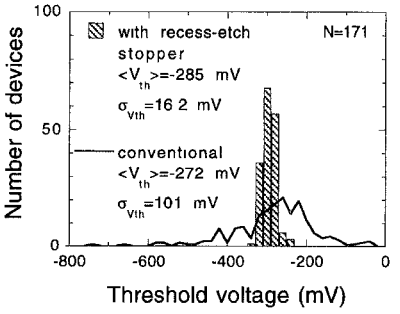


Fig. 2. Threshold voltage ($V_{\rm th}$) distribution (on a 2-in. wafer) for 0.1-μm-gate MOCVD-based HEMT's with an InP recess-etch stopper and for MBE-based ones without a recess-etch stopper.

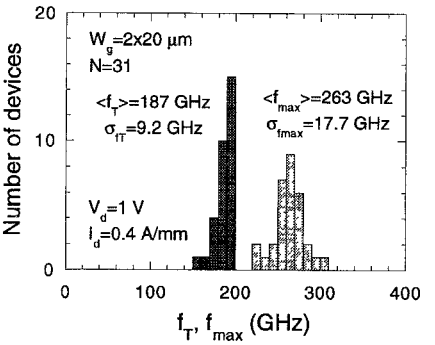


Fig. 3. Distribution (on a 2-in. wafer) of current-gain cutoff frequency (f_T) and maximum oscillation frequency ($f_{\rm max}$) for 0.1-μm-gate MOCVD-based HEMT's with an InP recess-etch stopper.

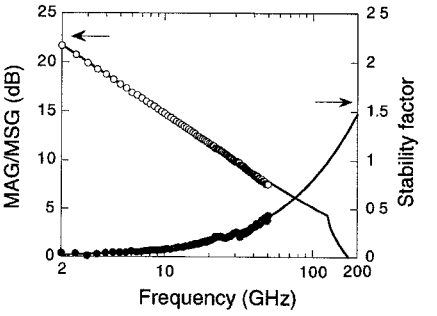


Fig. 4. Stability factor and maximum available/stable gain (MAG/MSG) of a InAlAs/InGaAs/InP HEMT with a 0.1-μm-long and 4 × 25-μm-wide gate at typical low-noise bias (V_{ds} = 0.75 V, V_{gs} = −0.2 V, and I_{ds} = 6.4 mA). The black and white circles show the measured stability factors and gains, respectively.

metal with air-bridge crossovers. Fig. 2 shows the threshold voltage ($V_{\rm th}$) distribution for the HEMT's on a 2-in. wafer. The distribution for conventional HEMT's without a recess-etch stopper is also shown for comparison. When using the conventional process, it is difficult to reduce the $V_{\rm th}$ standard deviation (σ) to less than 100 mV, but when using the InP recess-etch stopper σ can be reduced to 16 mV. The average transconductance was as high as 1.34 S/mm with a σ of 75 mS/mm. Fig. 3 shows the distribution of current-gain cutoff frequency (f_T) and maximum oscillation frequency ($f_{\rm max}$) estimated from measured S-parameters by −6 dB/octave extrapolation of current gain and Mason's unilateral power gain, respectively. Thirty-one of 32 samples of the HEMT's on a 2-in. wafer worked well and their average f_T and $f_{\rm max}$ values were very high, respectively 187 and 263 GHz (σ = 9.2 and 17.7 GHz, respectively). These results show that excellent yield and uniformity of the dc and rf characteristics are obtainable by the HEMT structure. In addition, these performance values are considered to be sufficient for application to high-yield small-scale integration for analog/digital IC's.

III. Circuit Design

A. Stabilization Technique for a Low-Noise Amplifier

Fig. 4 shows the frequency dependence of the stability factor (K) [23] and gain of a HEMT at typical low-noise bias. Although the HEMT has high maximum stable gain of 7.1 dB at 60 GHz, even at low-noise bias, the stability factor is less than unity up to more than 100 GHz. Therefore, some stabilization is necessary to design an amplifier even for millimeter-wave frequencies.

For the stabilization of a low-noise amplifier, negative feedback using pure reactance is suitable because it causes no degradation of the noise measure [24], [25] and consequently the infinite-stage noise figure (F_∞) [26]. Stabilization by series feedback using an inductive element between the source of an FET and the ground is the most suitable because it makes the optimum source impedance for the minimum noise and that for the maximum gain (i.e., impedance matching) close to each other [24], [27]. This technique has been applied to practical low-noise amplifiers [28]–[30] so as to improve input impedance matching. The magnitude of series inductive feedback, however, reduces as frequency decreases. Therefore, the stabilization tends to be shorter for the frequency band lower than the design band only by series inductive feedback.

Stabilization of an amplifier for low frequency bands has been performed by the frequency-dependent power-loss technique [29]–[32], [15]. This technique can stabilize an amplifier in frequencies other than the design band. However, the optimization of the stabilization by series inductive feedback in conjunction with the frequency-dependent power-loss technique has not yet been discussed in detail. In this section, we

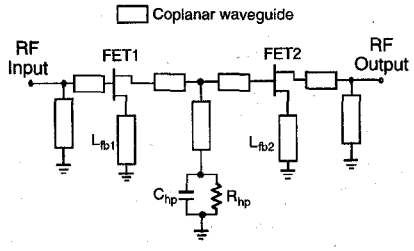
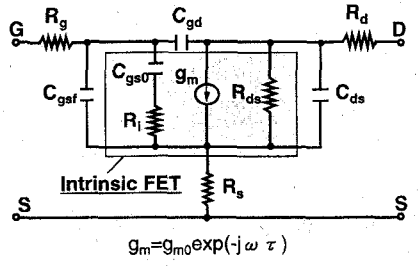


Fig. 5. Circuit diagram of low-noise amplifiers with series inductive feedback (L_{fb1} and L_{fb2}) and a frequency-dependent power-loss element (C_{hp} and R_{hp}). Stabilization methods in study are (a) series inductive feedback and frequency-dependent power loss, (b) only the feedback, and (c) only the power loss.



(a)

Device name	C_{gs0} (fF)	g_{m0} (mS)	R_i (Ω)	R_{ds} (Ω)	τ (ps)	Noise parameters at 60 GHz			
						F_{min} (dB)	R_n (Ω)	$\lvert\Gamma_{opt}\rvert$	$\angle\Gamma_{opt}$ (degree)
FET1	14.5	28	36	430	0.5	1.6	29	0.52	44
FET2	16.0	31	32	430	0.5	2.1	40	0.57	52

(b)

R_g (Ω)	R_s (Ω)	R_d (Ω)	C_{gsf} (fF)	C_{gd} (fF)	C_{ds} (fF)
2.0	6.4	10	9.3	9.3	0.4

(c)

Fig. 6. FET model and parameters for used in the stabillization study. The gate length and the width are 0.1 and 2×12.5 μm, respectively. (a) Equivalent circuit. (b), (c) Intrinsic and parasitic parameters, respectively.

evaluate the noise and gain tradeoff of an amplifier in which the stabilization method employs series inductive feedback and a frequency-dependent power-loss element. The focus is on the optimization for the design compromise between gain and noise.

Figs. 5 and 6 show the circuit diagram of two-stage amplifiers and the FET parameters used in this study. Because the power loss at the input of the first stage increases the amplifier noise much, power-loss element is inserted only between the stages. Fig. 7 shows the calculated gain dependence of F_∞ of an amplifier at 60 GHz employing (a) both series inductive negative feedback (L_{fb1} and L_{fb2}) and a frequency-dependent power-loss element (C_{hp} and R_{hp}), (b) only series inductive negative feedback, and (c) only a frequency-dependent power-loss element, shown in Fig. 5. The F_∞ is minimized for each gain point with the stability factor larger than unity for all frequencies. The widths of the center strip and the gap of the coplanar waveguide are 30 and 20 μm, respectively, for the input circuit, and 20 and 13 μm, respectively, for other

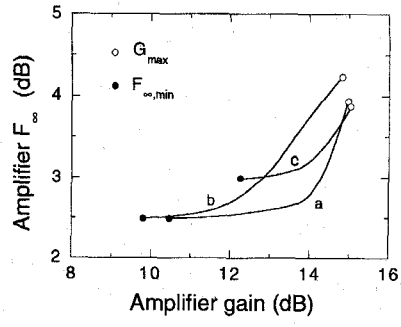
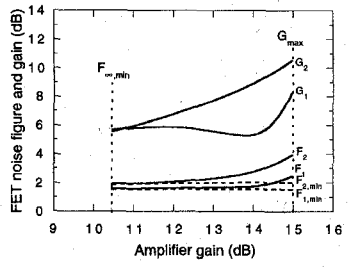
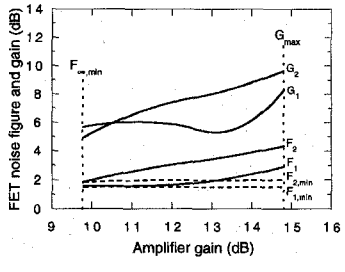


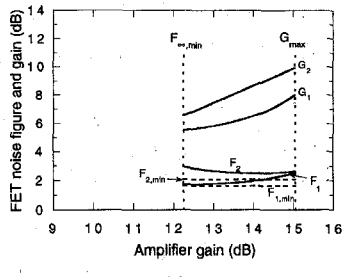
Fig. 7. Calculated gain dependency of the infinite-stage noise figure (F_∞) of two-stage amplifiers at 60 GHz using the stabilization methods (a)–(c) in Fig. 5. $F_{\infty,\min}$ and $G_{\max}$ are the values for the design minimizing F_∞ and the design maximizing the gain of the amplifier, respectively.



(a)



(b)



(c)

Fig. 8. Amplifier-gain dependency of the noise figure (F_1 and F_2) and gain (G_1 and G_2) of FET's in the first and second stages (FET1 and 2 in Fig. 5) of amplifiers using the stabilization methods (a)–(c) in Fig. 5. $F_{1,\min}$ and $F_{2,\min}$ are the minimum noise figures for FET1 and 2.

parts. The metal is 2-μm-thick plated gold. Fig. 7 shows that F_∞ for case (a) is the lowest for all possible gain. It also has small increase in F_∞ up to about three quarters of the possible gain range. To clarify the reason for this increase the noise figure and gain of the FET's in the first and second stage are examined as shown in Fig. 8(a)–(c) with the total amplifier gain as a parameter. These figures show that only case (a) can enable appropriate operation in gain and noise for each FET.

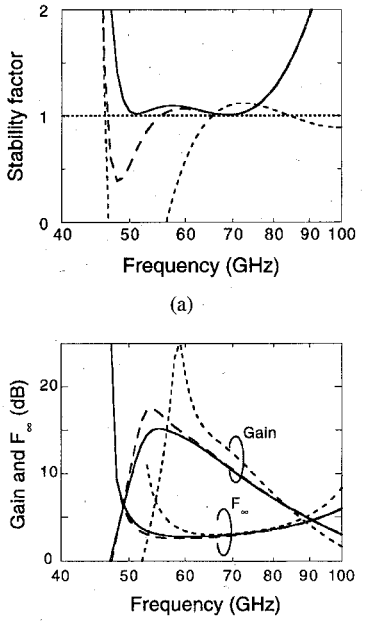


Fig. 9. Effect of series inductive feedback and frequency-dependent power-loss on stability, gain and F_∞ for an amplifier gain of 14 dB. Fine dotted, coarse dotted, and solid lines show the cases employing no stabillization, only series feedback, and both series feedback and power-loss element, respectively.

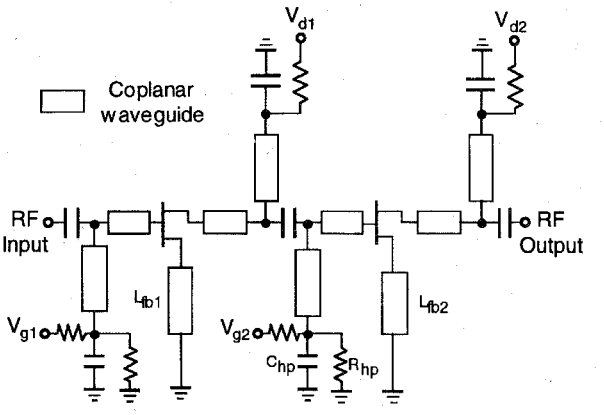


Fig. 10. Circuit diagram of the two-stage MMIC-LNA for fabrication.

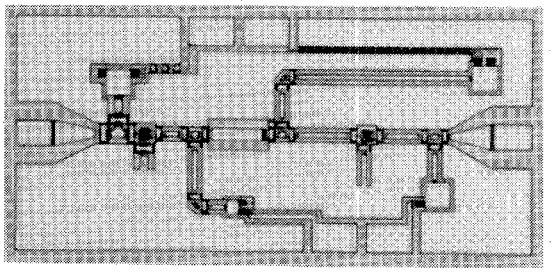


Fig. 11. Photomicrograph of a 60-GHz-band MMIC-LNA.

Fig. 9 shows a typical example how the stabilization in case (a) affects stability, gain, and F_∞ of an amplifier for a gain of 14 dB at 60 GHz. By series inductive negative feedback, the amplifier is stabilized at the design frequency of 60 GHz whereas a lower unstable region $(K < 1)$ remains. By adding frequency-dependent power-loss element, the unstable region is stabilized with little increase in F_∞ and decrease in gain at 60 GHz.

A two-stage MMIC-LNA was actually fabricated with stabilization using series inductive negative feedback and frequency-dependent power loss technique. The circuit configuration is modified from Fig. 5 to Fig. 10 so as to include a biasing function. The values of L_{fb1}, L_{fb2}, C_{hp}, and R_{hp} were optimized to minimize F_∞ for the designed gain. Capacitors other than C_{hp} are large enough to be regarded as shorts in millimeter-wave frequencies so as to simplify the impedance-matching design of the amplifier. Fig. 11 shows a photograph of the MMIC-LNA consisting of two 25-μm-wide-gate HEMT's with two gate fingers, I/O matching stubs for each stage using coplanar waveguides, and biasing circuits using MIM capacitors and resistors. The chip size is 1.8 × 0.8 mm. The design is based on the uniplanar circuit configuration [33], which enables circuits to be fabricated on one side of a substrate. This configuration is advantageous in the monolithic integration of microwave and digital circuits on one chip because the fabrication process of uniplanar MMIC's is compatible with that of the digital IC's.

B. Optimization of the Load Resistance of an SCFL Frequency Divider

In designing an ultrahigh-speed static frequency divider using InAlAs/InGaAs/InP HEMT's, we use the SCFL as a basic gate. This makes it possible to operate FET's almost within the saturation region of drain-current versus drain-voltage characteristics and thus avoids a decrease in the operation speed of FET's due to large gate-drain capacitance, which appears in the linear region. Fig. 12 shows the circuit diagram of the SCFL static frequency divider used in this study. It consists of an input buffer, a toggle flip-flop (T-FF), and an output buffer. The T-FF comprises master and slave D-latches. To increase the yield of the frequency divider, we control the load resistance (R_L) of the T-FF used to assure stable operation. The transit delay time due to the interconnection line and the charging time of FET fringe capacitance are neglected here to simplify discussion [34].

In the T-FF design, the logic swing is designed to be 0.7 V. Therefore, in the R_L region where the output voltage (V_{out}) of the T-FF is less than 0.7 V, the D-latch does not have an average gain of unity for a logic swing of 0.7 V. This means that the T-FF operates small-signal operation. In this region the toggle operation of the T-FF is unstable because a small change in FET parameters will decrease the logic swing or stop the toggle operation. In the R_L region where V_{out} is larger than 0.7 V, in contrast, the toggle operation is stable because it can tolerate for any FET-parameter change. Therefore, a larger R_L is preferable for stable operation of the frequency divider. The linear-response theory, however, predicts that the maximum toggle frequency $(f_{\text{tog,max}})$ is markedly decreased by increasing R_L.

According to linear-response theory as applied to SCFL gates [35], the delay $(\tau_{\text{CS-SF}})$ between the current switch (CS)

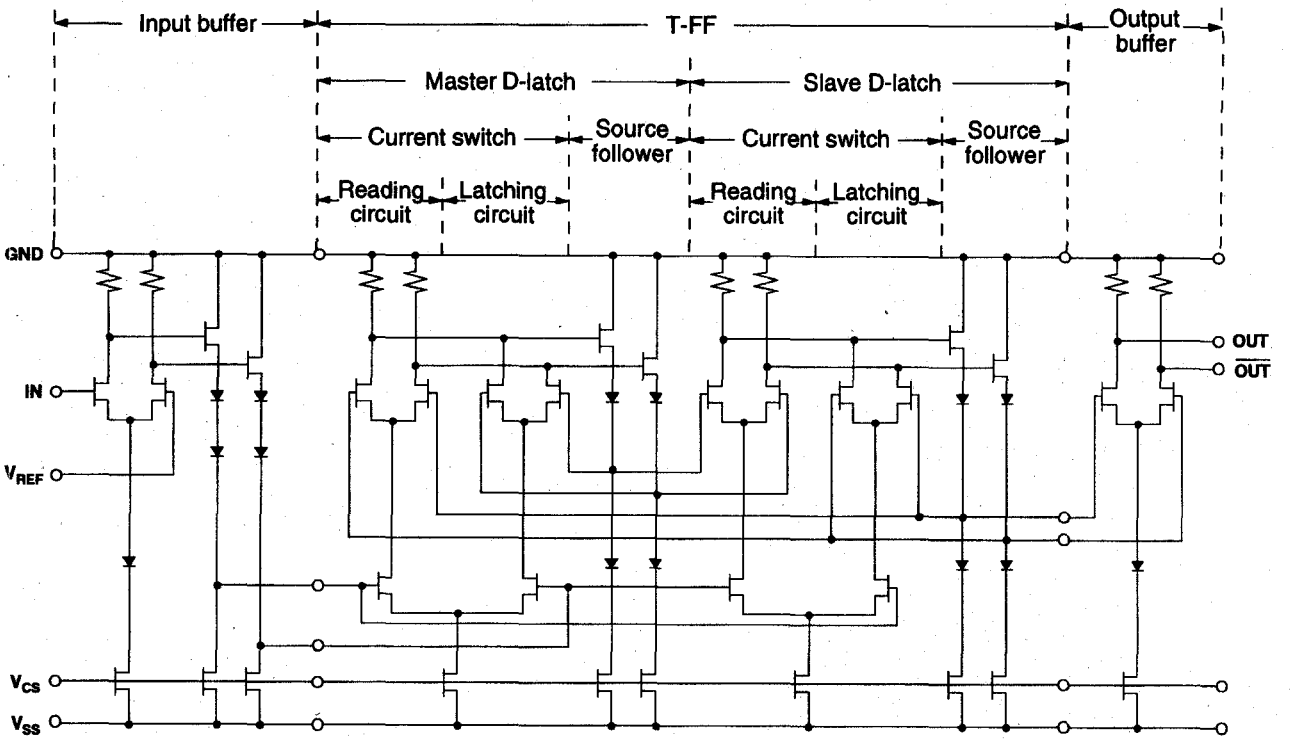


Fig. 12. Circuit diagram of a SCFL static frequency divider using toggle flip-flop (T-FF).

and the source follower (SF) circuit can be approximated as

$$\tau_{\text{SF-CS}} = R_L C_{gd} \tag{1}$$

where C_{gd} is the gate-drain capacitance of the HEMT. Similarly, by taking account of the input capacitance of a reading and latching circuit shown in Fig. 12 and including the mirror effect, the delay ($\tau_{\text{SF-CS}}$) between the SF and the CS can be approximated as

$$\tau_{\text{CS-SF}} = 2\frac{C_{gs} + (1 + G_v)C_{gd}}{g_{m,\max}} \tag{2}$$

where C_{gs} is the gate-source capacitance, $g_{m,\max}$ is the maximum transconductance, and G_v is the voltage gain of the CS. The G_v is expressed as

$$G_v = \langle g_m \rangle R_L \tag{3}$$

where $\langle g_m \rangle$ is the average transconductance. This results in the total delay time (t_{tot}) for a D-latch being

$$\tau_{\text{tot}} = 2\frac{C_{gs} + C_{gd}}{g_{m,\max}} + R_L C_{gd}\left(1 + 2\frac{\langle g_m \rangle}{g_{m,\max}}\right). \tag{4}$$

For a short-gate-length HEMT, such as the one used in this study, the second term of this equation is almost the same as or much larger than the first term. Therefore, according to the linear-response theory, the gate delay for a D-latch monotonically increases (i.e., $f_{\text{tog,max}}$ decreases) as R_L increases.

To examine the effect of nonlinearity, on the other hand, transient circuit simulation was carried out using the Hewlett-Packard Microwave Design System [36]. Fig. 13 shows the calculated $f_{\text{tog,max}}$ and V_{out} of the T-FF. The R_L dependency of $f_{\text{tog,max}}$ in Fig. 13 is weak, suggesting that the nonlinear effect shortens the effective delay time in a D-latch. This nonlinear effect probably originates from waveform re-shaping due to clipping the amplitude higher than the gate voltage specified by the current source FET. The frequency divider can operate stably (i.e., $V_{\text{out}} > 0.7$ V) for R_L larger than 84 Ω as shown in Fig. 11. Therefore, we chose an R_L value of 113 Ω taking into account the R_L margin of 26%.

With the R_L value determined as described above, an SCFL static frequency divider was designed and fabricated. To ensure high-speed operation, we paid the most attention to minimize the signal path length so as to reduce the signal transit delay through interconnection lines [34]. In addition, the impedance matching between the output impedance of an FET and the characteristic impedance of an interconnection line is important because large impedance mismatch causes serious multireflection delay. Delay-time analysis considering the distributed effect mentioned above and fringe capacitance of FET's showed that the optimum gate width for high-speed operation was 20 μm. Fig. 14 shows a microphotograph of the frequency divider. It consists of 32 FET's, 14 Schottky diodes, eight resistors, and five metal–insulator–metal (MIM) capacitors. The chip size is 1.25 × 1.0 mm, and the gate widths of the FET's for the input buffer, the T-FF, and the output buffer were, respectively, 50, 20, and 20 μm. The resistor comprises mesa-isolated modulation-doped heterostructure with ohmic metal for both terminals. The sheet and contact resistance used

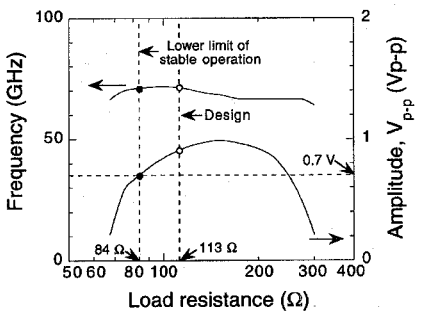


Fig. 13. Load resistance dependency of maximum toggle frequency of a D-latch and signal amplitude at the output of T-FF ($V_{ss} = -4$ V and $V_{cs} = 0.2$ V).

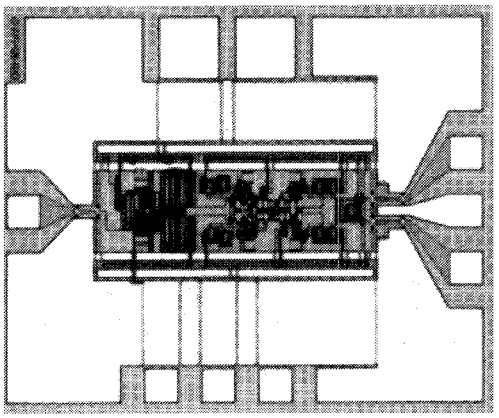


Fig. 14. Photomicrograph of a frequency-divider IC.

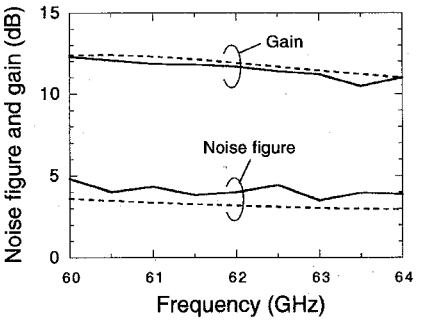


Fig. 15. Designed (dashed lines) and measured (solid lines) frequency dependency of noise figure and gain of an MMIC-LNA ($V_{d1} = 1.07$ V, $V_{d2} = 0.95$ V, $V_{g1} = V_{g2} = -0.11$ V, $I_{d1} = 7.2$ mA, $I_{d2} = 3.4$ mA, $I_{g1} = -0.82$ mA, and $I_{g2} = 0.81$ mA).

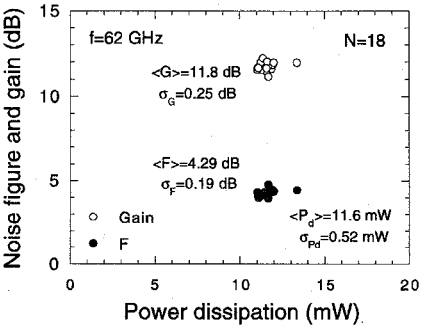


Fig. 16. Distribution of noise figure (F), gain (G), and power dissipation (P_d) for MMIC-LNA's on a 2-in. wafer ($V_{d1} = 1.07$ V, $V_{d2} = 0.95$ V, and $V_{g1} = V_{g2} = -0.11$ V).

in the design were 130 Ω/sq. and 0.07 Ωmm, respectively. Because the maximum current for R_L in the design is 13.6 mA and the current capacity of a resistor is 0.5 mA/μm, the width and length of R_L were determined to be 27 and 22.5 μm, respectively.

IV. IC Performance

A. MMIC-LNA

Sixty-GHz-band two-stage MMIC-LNA's were fabricated in order to examine the applicability of the HEMT-IC process to analog IC's. The circuit design has been described in Section III-A, and Fig. 15 shows that the designed and measured values of noise figure (F) and gain agree well. Between 60 and 64 GHz, the LNA showed a low average F of 4.1 dB and a high average gain of 11.5 dB. This low-noise and high-gain performance is due to the stability optimization performed as well as the excellent noise and gain performance of the HEMT's. Fig. 16 shows the distribution of F, gain, and power dissipation for LNA's fabricated on a 2-in. wafer. At 62 GHz the average F and gain were respectively 4.3 and 11.8 dB, with extremely small σ values of 0.19 and 0.25 dB, respectively. This uniformity is also due to the uniformity of the HEMT's. For 24 samples on a 2-in. wafer, the yield was 75%.

B. Frequency Divider

The SCFL static binary frequency dividers described in Section III-B were fabricated in order to examine the applicability of the HEMT-IC process to digital IC's. The fabrication process was the same as the process used for fabricating the MMIC-LNA's. The average sheet and contact resistance of the fabricated wafer were, respectively, 108 Ω/sq. and 0.075 Ωmm, with σ values of 3.04 Ω/sq. and 0.010 Ωmm, respectively. From these values the average R_L was calculated to be 95 Ω with a σ of 2.6 Ω. Accordingly, the 3σ criteria for minimum R_L was 87 Ω, which is within the stable-operation range for a frequency divider as described in Section III-B. The performance of the fabricated frequency dividers is shown in Fig. 17. Although the interconnection-line process is not yet optimized for digital IC's and delays due to the interconnections are consequently still large [34], the average maximum toggle frequency on a 2-in. wafer reached 36.7 GHz with a σ of only 0.55 GHz. The average power dissipation was 610 mW with a σ of 47 mW. The yield for 16 samples on a 2-in. wafer was 63%. This high yield and uniformity are partly due to the stability-oriented R_L-design method described in Section III-B. From the yield of the frequency dividers, the yield for an FET was calculated to be 98.6%, assuming that the yield of the frequency divider depends only on FET's and the yields of FET's are independent of each other. This result agrees well with the high yield of the discrete HEMT's described in Section II.

V. Conclusion

The applicability of the 0.1-μm-gate InAlAs/InGaAs/InP HEMT process to analog/digital IC's has been examined.

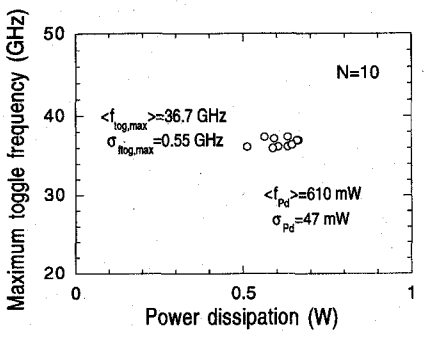


Fig. 17. Distribution of the maximum toggle frequency ($f_{\mathrm{tog,max}}$) versus power dissipation (P_d) for frequency dividers on a 2-in. wafer ($V_{ss} = -4$ V, $V_{cs} = 0.2$ V, and $V_{\mathrm{in}} = 0.45$ V).

The HEMT with a T-shaped-gate and InP recess-etch stopper showed excellent uniformity. An MMIC-LNA and an SCFL static frequency divider were designed with the top design priorities on stable operation, high yield, and uniformity. In designing the MMIC-LNA, the stabilization was optimized so as to minimize noise for all designable gain while maintaining stability for all frequencies. The MMIC-LNA showed a yield of 75% and at 62 GHz had a noise figure of 4.3 ± 0.19 dB and a gain of 11.8 ± 0.25 dB. In designing the frequency divider, load resistance was optimized for stable and high-speed operation. The frequency divider showed a yield of 63% and had a maximum toggle frequency of 36.7 ± 0.55 GHz. These results show that the monolithic integration of both analog and digital circuits onto one chip by using this HEMT process is both feasible and promising.

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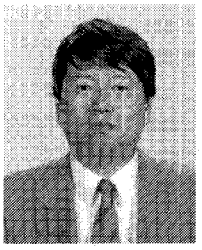

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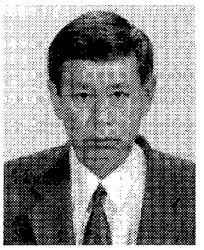

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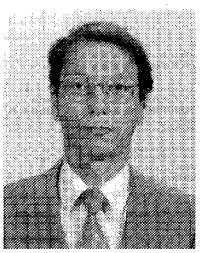

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